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Design of High-speed, Low-power FIR Filters with Fine-grained Cost Metrics

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A Continuous-Time ADC/DSP/DAC System With No Clock and With Activity-Dependent Power Dissipation

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Input-specific Dynamic Power Optimization for VLSI Circuits

Fei Hu; Agrawal, V.D.;

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A 2.4-GHz monolithic fractional-N frequency synthesizer with robust phase-switching prescaler and loop capacitance multiplier

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Inertial and degradation delay model for CMOS logic gates

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Transition analysis on FPGA for multiplier-block based FIR filter structures

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Publication Title

- ☐ Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on (1)
- ☐ Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on (1)
- ☐ Defect and Fault Tolerance in VLSI Systems, 2004. DFT 2004. Proceedings. 19th IEEE International Symposium on (1)
- ☐ Computer Design: VLSI in Computers and Processors, 2005. ICCD 2005. Proceedings. 2005 IEEE International Conference on (1)
- ☐ Circuits and Systems, 2005. 48th Midwest Symposium on (1)
- ☐ Circuits and Systems, 2006. APCCAS 2006. IEEE Asia Pacific Conference on (1)
- ☐ Low Power Electronics and Design, 2006. ISLPED'06. Proceedings of the 2006 International Symposium on (1)

Subject

- ☐ Components, Circuits, Devices & Systems (7)
- ☐ Communication, Networking & Broadcasting (4)
- ☐ Engineered Materials, Dielectrics & Plasmas (3)
- ☐ Computing & Processing (Hardware/Software) (1)
- ☐ Photonics & Electro-Optics (1)
- ☐ Signal Processing & Analysis (1)
- ☐ General Topics for Engineers (Math, Science & Engineering) (1)

Conference Country

- ☐ Switzerland (1)
- ☐ Lebanon (1)

Conference Location

- ☐ Singapore (1)
- ☐ Geneva (1)
- ☐ Jounieh (1)
- ☐ Covington, KY (1)
- ☐ Tegernsee (1)

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